Calculating Differential Impedance of Parallel PCB Traces Without Ground Plane

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The Problem

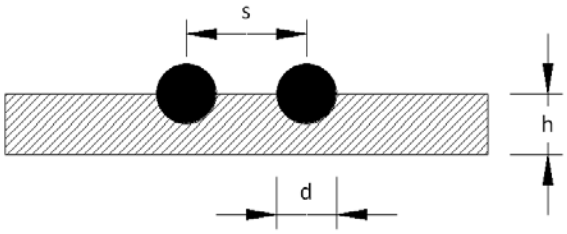
While facing a recent design challenge, I came upon the need to calculate the differential impedance of a pair of traces on a circuit board when no ground plane was present. A few days searching the Internet turned up very little relevant information. I did locate one ridiculously complicated formula that used elliptic integrals of the first kind, which to be honest, was way over my head. I needed something simple.

Parallel Wires

Fortunately there was a good place to start. A long time ago somebody worked out a very good approximation for the impedance of a pair of parallel (or twisted pair) wires in a dielectric. It is given as:

$$Z_o = \left(\frac{120}{\sqrt{\varepsilon_{eff}}} \right) \cdot \ln\left(\frac{2s}{d} \right)$$

We can modify this a bit closer to our desired result by enclosing half of the cross section in a dielectric of ε_r. The inductance of the traces will not change, but capacitance will increase, thereby lowering impedance.



Half of the electric fields are in air, the other half in dielectric. Therefore, the effective permittivity will be:

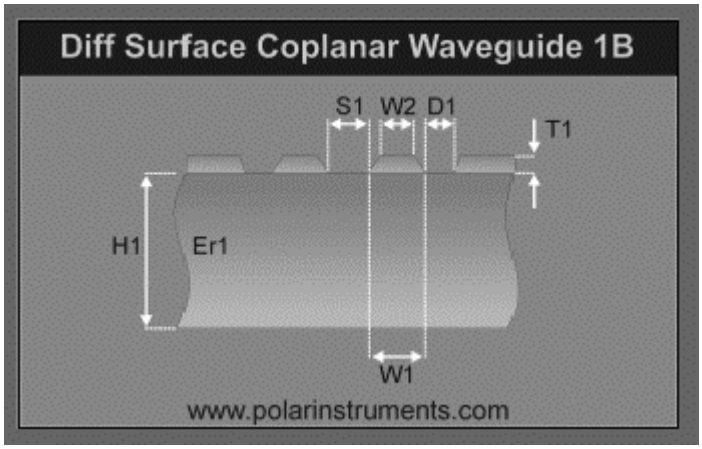
$$\varepsilon_{eff} = \frac{1}{2} + \frac{\varepsilon_r}{2} = \frac{(\varepsilon_r + 1)}{2}$$

However, two problems remain. One is that the PCB is not infinitely thick. The other is that PCB traces are not round.

Simulators

The obvious solution to this problem is to employ one of the many electro-magnetic simulators available. But we don't all have access to one! And they can be rather

expensive. Fortunately, I was lucky to get a 15-day evaluation license for the Si8000 simulator from Polar Instruments. With this handy tool I was able to easily calculate results for many conditions. It was based on these data that I reverse engineered an approximate formula.



PCB Thickness

The first challenge was how to deal with the effective permittivity due to finite thickness of the PCB. We know it should range from 1.00 to $(\varepsilon_r + 1)/2$ as the thickness goes from zero to very thick. But what function to use? While browsing through my 35 year old CRC Handbook, I found the arctangent() to have just the right properties. For positive values the arctangent goes from zero to $\pi/2$. It was a simple matter of scaling the amplitude and adding an offset of 1.00 to get a working result. It simplified to:

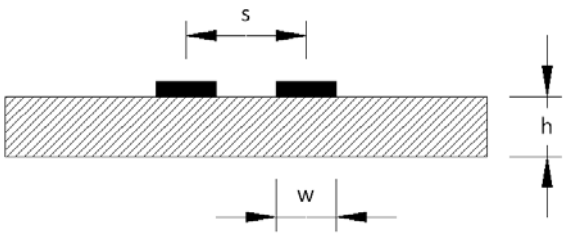
$$\varepsilon_{eff} = 1 + \left(\frac{\varepsilon_r - 1}{\pi}\right) \cdot \arctan\left(\frac{\eta \cdot h}{w}\right)$$

Flat Conductors

Given the physical similarities to the round wire configuration, the new formula takes the same form:

$$Z_o = \left(\frac{\chi}{\sqrt{\varepsilon_{eff}}}\right) \cdot \ln\left(\frac{2s}{w}\right)$$

With a focus on low cost, this analysis optimizes results based on FR4 ($\varepsilon_r = 4.3$) material with realistic conductor sizes and spacing.



Using a conductor width of 20 mils and a spacing of 50 mils, the simulator gave an impedance of 256 ohms in air. With a PCB thickness of 63 mils, the result was 163 ohms. Using a little algebra and (2s/w) = 5, the value of χ can be calculated as roughly 160. We now have the result:

$$Z_o = \left(\frac{160}{\sqrt{\varepsilon_{eff}}} \right) \cdot \ln\left(\frac{2s}{w} \right)$$

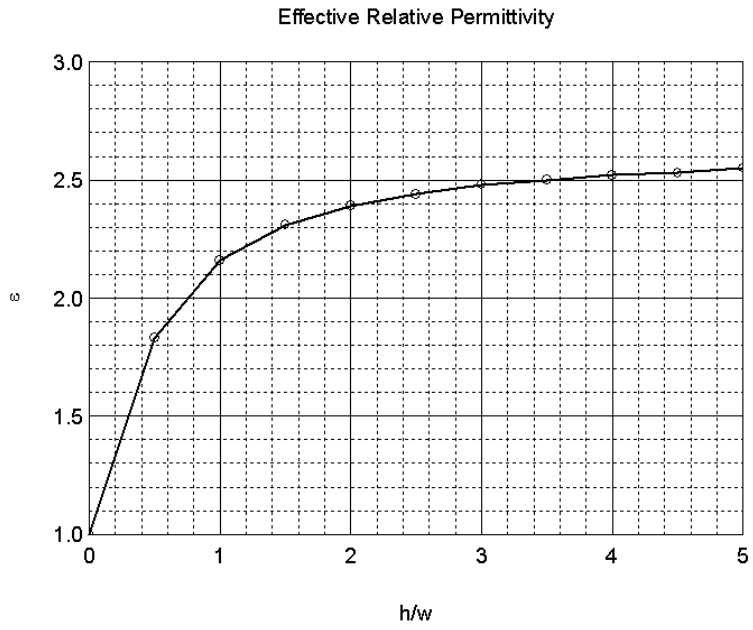
Now we just need to curve fit the dielectric. The endpoints are already correct, with ε_{eff} of either 1.00 or $(\varepsilon_r + 1)/2$. Using the 163 ohms result from the above conditions, we obtain that ε_{eff} must be 2.50. Rearranging our ε_{eff} formula, η can be calculated as:

$$\eta = \frac{w}{h} \cdot \tan\left[\frac{\pi\left(\varepsilon_{eff} - 1\right)}{\varepsilon_r - 1} \right] = 2.2$$

Rounding off to simplify things, we end up with the approximation of:

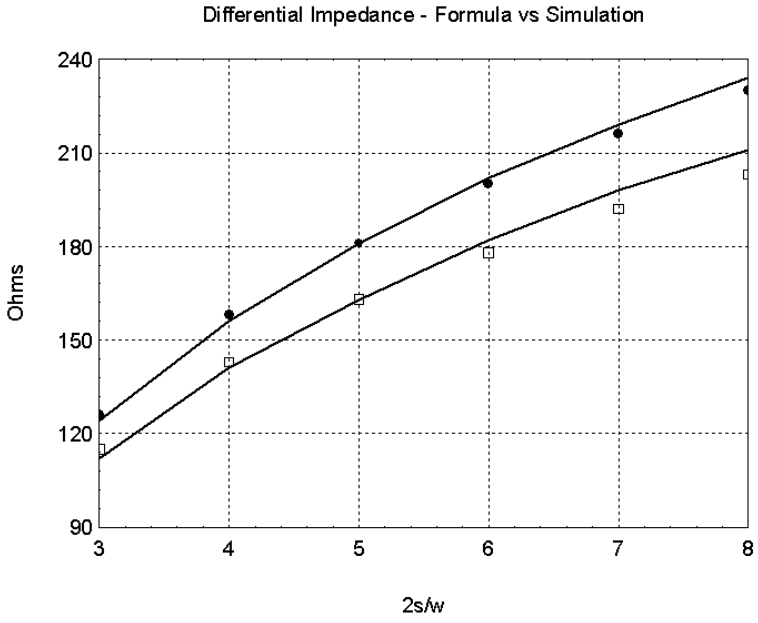
$$\varepsilon_{eff} = 1 + \left(\frac{\varepsilon_r - 1}{\pi} \right) \cdot \arctan\left(\frac{2h}{w} \right)$$

This was plotted for an FR4 circuit board as a function of the thickness to trace width.

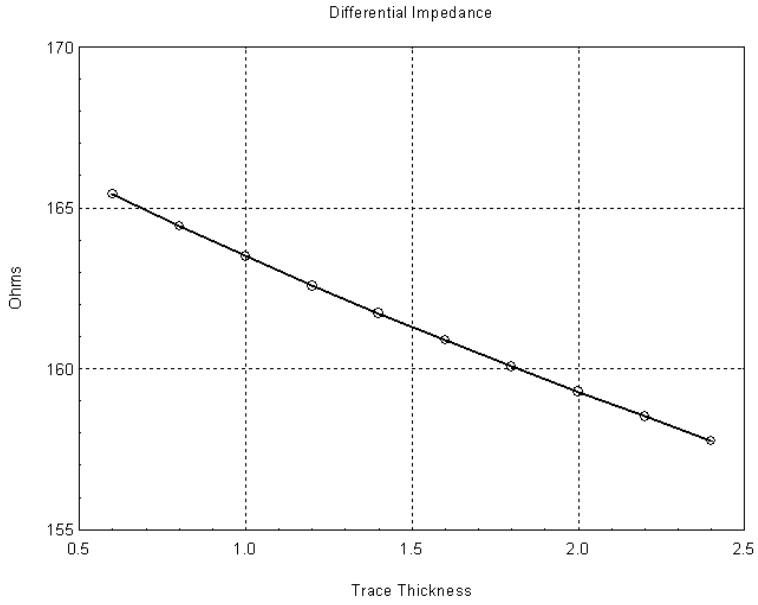


Results

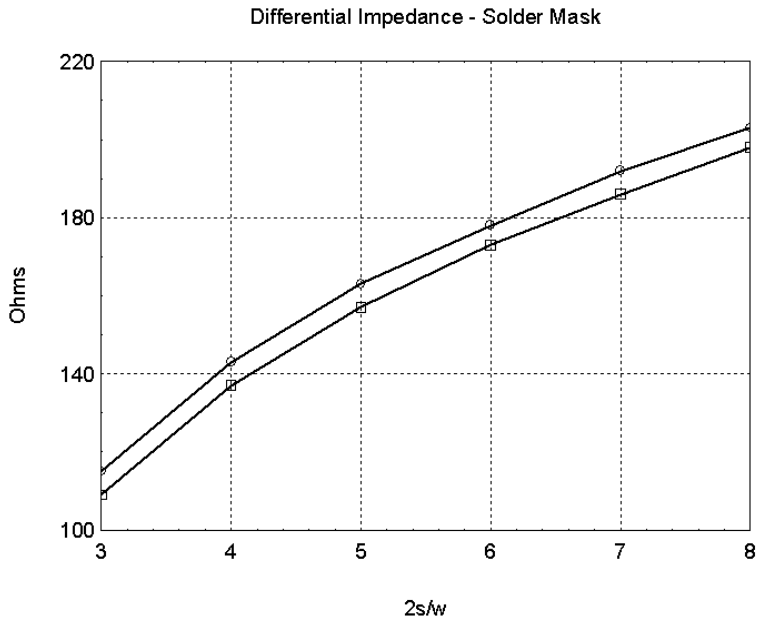
The following plot shows the calculated versus simulated results for two different board examples. The lower trace is our 63 mil thick FR4 board; the upper is for a Rogers 4003 ($\varepsilon_r = 3.55$) 30 mil thick board. The formula gives surprisingly accurate results with an error of only a few percent over this useful range.



Oh, I forgot to mention, this analysis is based on 1 ounce copper, or a trace thickness of 1.2 mils. Simulations were run to test the sensitivity of this parameter.



The effect of solder mask was also investigated, which had a similar effect, decreasing the impedance. The lower trace is with solder mask.



Conclusion

This newly derived empirical formula provides very good estimates of impedance over a wide range of conditions and materials. I found it very useful for optimizing the "feed" for my circuit board antenna project.